WHAT IS CLAIMED IS:

1. A stream routing unit for routing each of a plurality of input packet streams to any of a plurality of destinations, the stream routing unit comprising:

a plurality of input ports for receiving respective input streams;

a plurality of output ports associated with respective destinations to which the input packet streams can be routed;

storage means for holding packets of the input packet streams at addressable locations each identifiable by an address;

an assignment data structure identifying for each input stream at least one destination to which each input packet stream is to be routed; and

a packet allocation data structure holding for each new incoming packet a source identifier identifying the origin of the packet and the address in the storage means where the packet is held, the packet allocation data structure further holding information identifying the intended destination of the packet derived from the assignment data structure.

2. The stream routing unit according to claim 1, wherein the input packet streams have a lower bit rate than output streams into which they are merged at the plurality of output ports.

3. The stream routing unit according to claim 1, wherein the assignment data structure is a matrix.

4. The stream routing unit according to claim 1, wherein the packet allocation data structure is an array of slots, each slot holding a source identifier and associated address.

5. The stream routing unit according to claim 4, wherein the packet allocation data structure is associated with a write pointer which is configured to point to the next available slot in the array for the source identifier and address of the next incoming packet.

6. The stream routing unit according to claim 4, wherein information identifying the intended destination of the packet is provided by a set of destination pointers, each destination pointer associated with a respective output port and each destination pointer being configured to point to a slot in the array which holds a source identifier and address of a packet intended for a particular destination associated with a particular output port.

7. The stream routing unit according to claim 1, wherein the packets of a said input stream are of a common length.

8. A data communication system for routing incoming packets to at least one destination, the system comprising:

a plurality of packet stream sources each generating a packet stream;

a stream routing unit comprising:

a plurality of input ports for receiving respective input packet streams;

a plurality of output ports associated with respective destinations to which the input packet streams can be routed;

storage means for holding packets of the input packet streams at addressable locations each identifiable by an address;

an assignment data structure identifying for each input stream at least one destination to which each input packet stream is to be routed; and

a packet allocation data structure holding for each new incoming packet a source identifier identifying the origin of the packet and the address in the storage means where the packet is held, the packet allocation data structure further holding information identifying the intended destination of the packet derived from the assignment data structure; and

a plurality of destinations for receiving packets of the packet streams generated by the sources.

9. The data communication system according to claim 8, wherein at least one of the destinations comprises a programmable transport interface.

10. The data communication system according to claim 8, wherein the input packet streams have a lower bit rate than output streams into which they are merged at the plurality of output ports.

11. A method of routing packet streams from a plurality of sources to any of a plurality of destinations, the method comprising:

receiving said packet streams;

identifying for each input packet stream at least one destination to which each input packet stream is to be routed using an assignment data structure;

holding each packet of the packet stream at an addressable location identifiable by an address in a storage means;

holding for each new incoming packet a source identifier identifying the origin of the packet and the address in the storage means where the packet is held;

holding information identifying the intended destination of the packet derived from the assignment data structure; and

using said information identifying the intended destination to route the packet from the storage means to the or each output port associated with the respective identified destination(s).

12. The method according to claim 11, wherein the input packet streams have a lower bit rate than output streams into which they are merged at the output ports.

13. The method according to claim 11, wherein said information identifying the intended destination of the packet is provided by a set of destination pointers, said method further comprising:

associating each destination pointer with a respective output port; and

configuring each destination pointer to point to a source identifier and address of a packet intended for the destination associated with that output port.

14. The method according to claim 11 further comprising:

holding each new incoming packet in a packet allocation data structure having a plurality of slots;

holding in each slot a source identifier and associated address; and

associating each slot with a write pointer which is configured to point to the next available slot in the array for the source identifier and address of the next incoming packet.

15. A device for delivering incoming packets to at least one destination, the device comprising:

a source to destination matrix for mapping at least one source to at least one destination;

a packet allocation table for associating a source and at least one destination for a particular packet with a memory location at which the particular packet is stored; and

an algorithm for controlling removal of the incoming packets from a memory to at least one destination, wherein the incoming packets have a lower bit-rate than packets delivered to the at least one destination.

16. The device of claim 15 further comprising a memory for holding the incoming packets at addressable locations each identifiable by an address.

17. The device of claim 15 further comprising:

a plurality of input ports for receiving respective input packets; and

a plurality of output ports associated with respective destinations to which the input packets can be routed.

18. A method for delivering incoming packets to at least one destination, the method comprising:

mapping at least one source to at least one destination;

associating a source and at least one destination for a particular packet with a memory location at which the particular packet is stored; and

controlling removal of the incoming packets from a memory to at least one destination, wherein the incoming packets have a lower bit-rate than packets delivered to the at least one destination.

19. The method of claim 18 further comprising holding the incoming packets at addressable locations each identifiable by an address.

20. The method of claim 18 further comprising:

receiving respective input packets; and

routing outgoing packets through a plurality of output ports associated with respective destinations.

21. The method of claim 18, wherein mapping further comprises creating a source to destination matrix.

22. The method of claim 18, wherein the at least one destination is a programmable transport interface.

23. The method of claim 18, wherein the memory is an SRAM memory.

24. A method for controlling removal of packets from a memory to at least one destination, the method comprising:

reading each packet from a memory;

determining if each packet is destined for more than one destination;

if the packet is destined for more than one particular destination, outputting the packet when a port for each particular destination is available; and

if the packet is destined for one particular destination, outputting the packet only when a port for the particular destination is free.

25. The method of claim 24 further comprising forming an array for indicating, for each packet, a source and destination for a packet held in a particular memory location.

26. The method of claim 25 further comprising assigning, for each destination, a pointer directed at a particular slot of the array.

27. The method of claim 24 further comprising assigning a write pointer to point to a next available slot in the array.

28. An apparatus for controlling removal of packets from a memory to at least one destination, the apparatus comprising:

a processor for reading each packet from a memory and determining if each packet is destined for more than one destination; and

a plurality of outputs for receiving the packet, wherein if the packet is destined for more than one particular destination, the plurality of outputs receiving the packet when a port for each particular destination is available.

29. The apparatus of claim 28 further comprising an array for indicating, for each packet, a source and destination for a packet held in a particular memory location.

30. The apparatus of claim 29 further comprising a pointer, assigned for each destination, directed at a particular slot of the array.

31. The apparatus of claim 28 further comprising a write pointer for pointing to a next available slot in the array.